



WINSTAR Display Co.,Ltd.
華凌光電股份有限公司

2.9 inch E-paper Display Series

WAA0290A2ADA8NXXX000

Product Specifications

Customer	Standard
Description	2.9" E-PAPER DISPLAY
Model Name	WAA0290A2ADA8NXXX000
Date	2024/09/26
Revision	1.0

	Design Engineering		
	Approval	Check	Design

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REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	SEP.26.2024	New Creation	ALL	

1. Over View

WAA0290A2ADA8NXXX000 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black full display capabilities. The 2.9 inch active area contains 296×128 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT , VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2.Features

296×128 pixels display
 High cntrast High reflectance
 Ultra wide viewing angle Ultra low power consumption
 Pure reflective mode
 Bi-stable display
 Commercial temperature range
 Landscape portrait modes
 Hard-coat antiglare display surface
 Ultra Low current deep sleep mode
 On chip display RAM
 Waveform can stored in On-chip OTP or written by MCU
 Serial peripheral interface available
 On-chip oscillator
 On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
 I2C signal master interface to read external temperature sensor
 Built-in temperature sensor

3.Mechanical Specifications

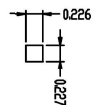
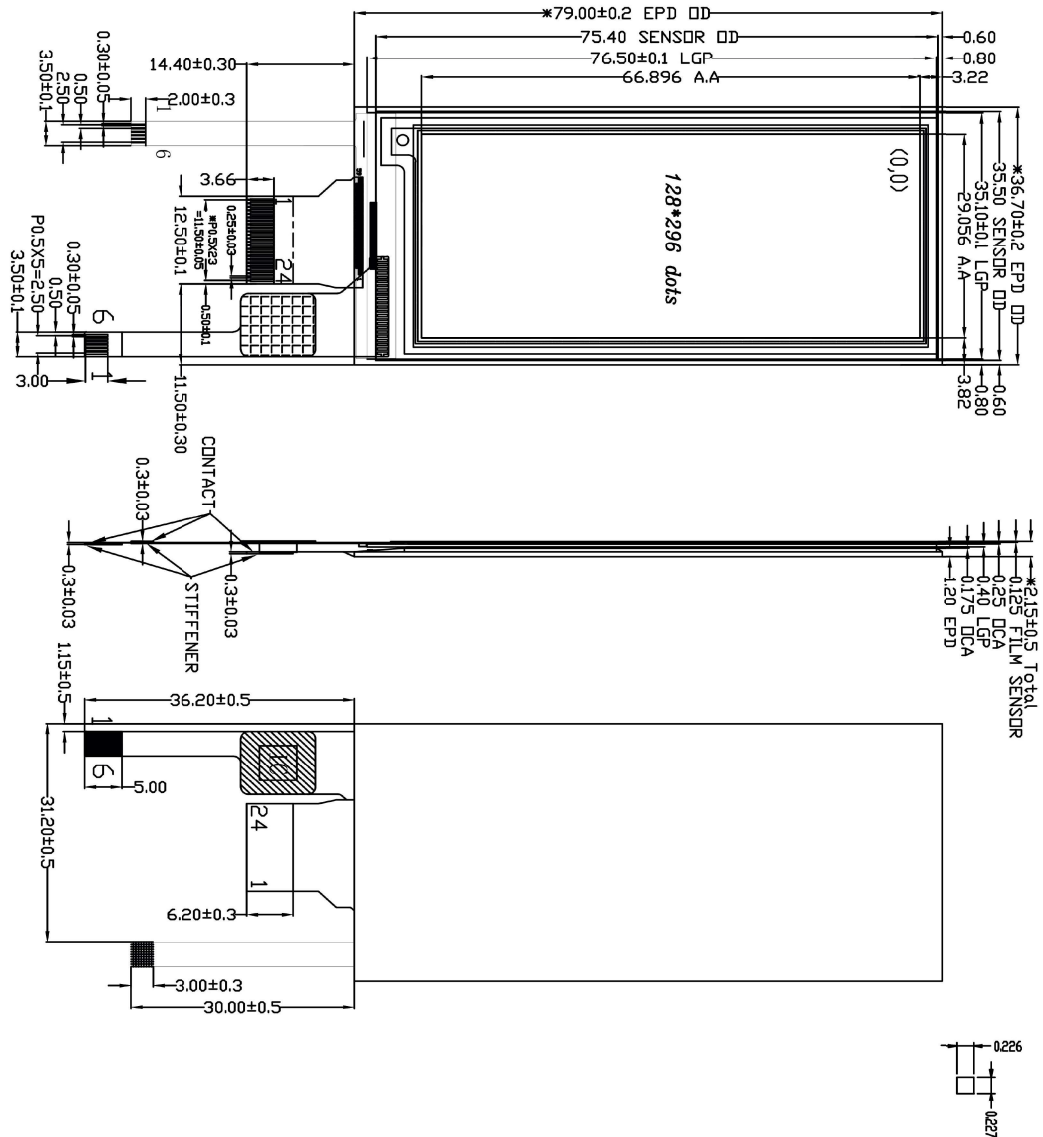
Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	296 (H)×128(V)	Pixel	Dpi:112
Active Area	29.056(H)×66.896(V)	mm	
Pixel Pitch	0.227×0.226	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H)×79.0(V) ×1.2(D)	mm	
Weight	5.5±0.5	g	

4. Mechanical Drawing of EPD module

CUSTOMER'S APPROVED:

DATE:

PAGE: 1/1



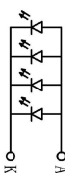
CTP pin

PIN NO.	Symbol
1	GND
2	INT(3.3V)
3	RST(3.3V)
4	VDD(3.3V)
5	SCL(3.3V)
6	SDA(3.3V)

EPD pin

PIN NO.	Symbol
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSL
7	TSDA
8	BS1
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCOM

LED CIRCUIT DIAGRAM
(LED 1*4=4 DIES)



Vf=2.75V min 2.9V typ 3.0V max
If=60mA

1	Display mode	EPD_B/W
2	Resolution ratio	2.9" 128*296
3	Operating Voltage:	VCI=3.0V
4	Operating Temp:	0°C~50°C
5	Storage Temp:	-25°C~70°C
6	controller/driver:	SSD1680
7	CTP controller/driver	F76336U
8	Unspecified tolerance:	±0.2
9	Customer No.:	
10	Dimensions with mark "*" are important	
11	RoHS compliant	

5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU

communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When

the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	°C
Storage Temp range	TSTG	-25 to+70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V _{SS}	-		-	0	-	V
Logic supply voltage	V _{CI}	-	V _{CI}	2.2	3.0	3.7	V
Core logic voltage	V _{DD}		V _{DD}	1.7	1.8	1.9	V
High level input voltage	V _{IH}	-	--	0.8 V _{CI}	--	-	V
Low level input voltage	V _{IL}	-	--	-	--	0.2 V _{CI}	V
High level output voltage	V _{OH}	I _{OH} = - 100uA	--	0.9 V _{CI}	9	-	V
Low level output voltage	V _{OL}	I _{OL} = 100uA	--	--		0.1 V _{CI}	V
Typical power	P _{TYP}	V _{CI} = 3.0V	--	--		--	mW
Deep sleep mode	P _{STPY}	V _{CI} = 3.0V		--	0.003	--	mW
Typical operating current	I _{opr} _V _{CI}	V _{CI} = 3.0V		-	3.0	--	mA
Full update time	--	25 °C			3		sec
Fast update time	-	25 °C			1.5		sec
Partial refresh time		25 °C			0.3		sec
Sleep mode current	I _{slp} _V _{CI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	I _{dslp} _V _{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes:

1) Refresh time: the time it takes for the whole process from the screen change to the screen stabilization.

2) The difference between different refresh methods:

Full refresh: The screen will flicker several times during the refresh process;

Fast Refresh: The screen will flash once during the refresh process;

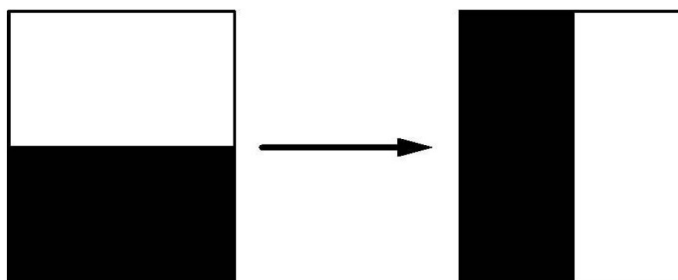
Partial refresh: The screen does not flicker during the refresh process.

During the fast refresh or partial refresh of the electronic paper, it is recommended to add a full-screen refresh after 5 consecutive operations to reduce the accumulation of afterimages on the screen.

1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.

2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by WINSTAR Display.



6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.3.2 MCU Serial Interface (4-wire SPI)

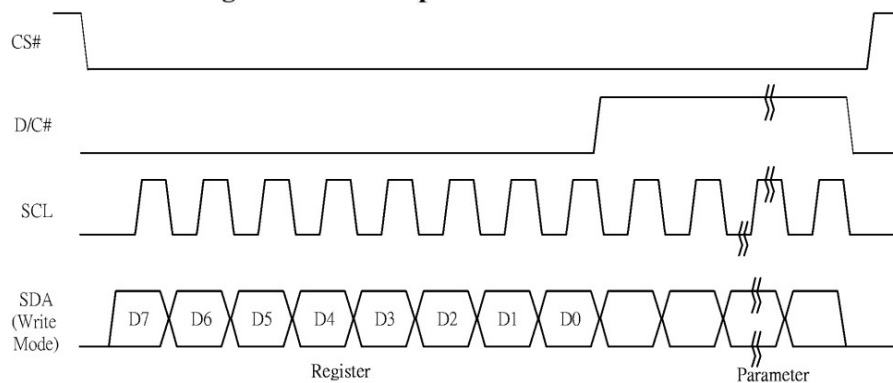
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

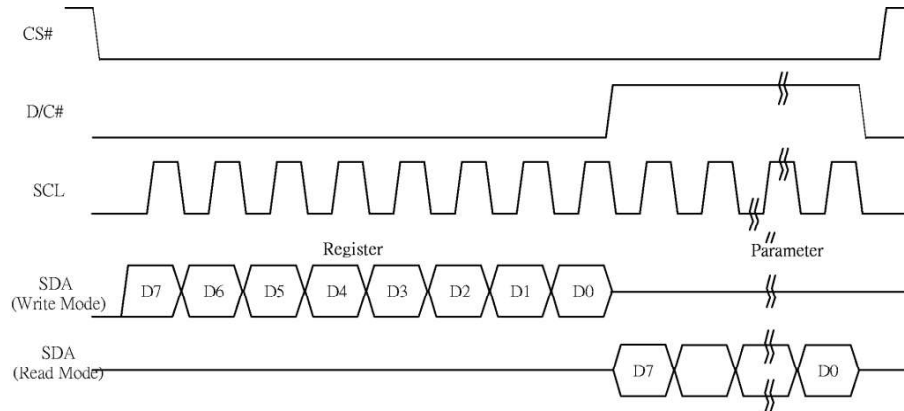
In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode


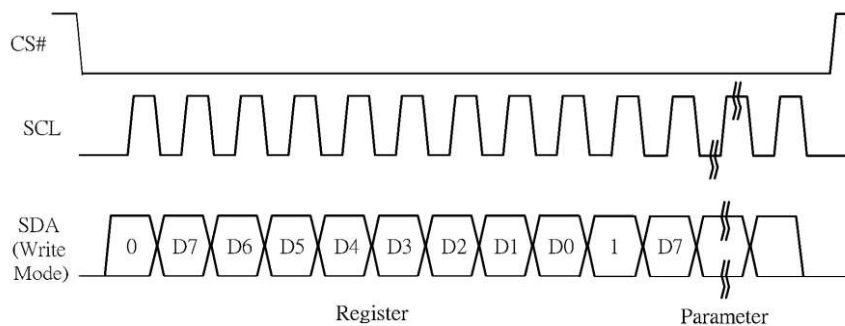
6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

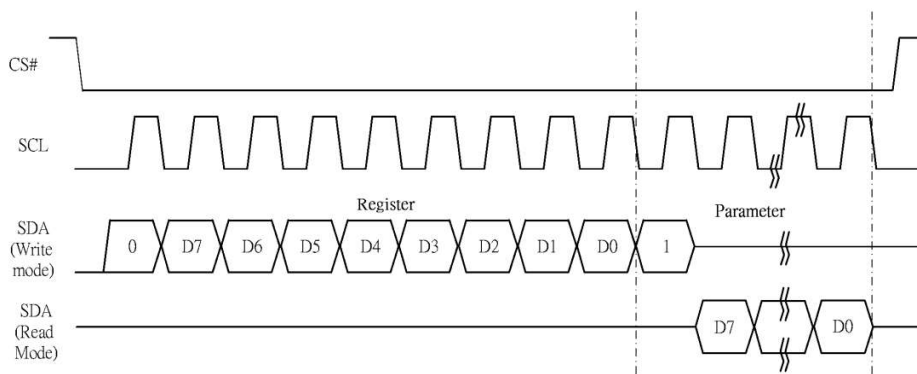
Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

Figure 6-3: Write procedure in 3-wire SPI mode


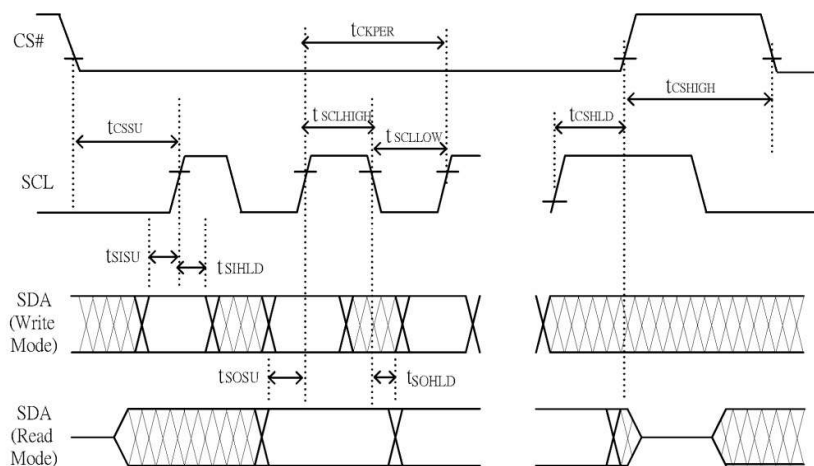
In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode


6.3.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.


Changed Diagram

Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Write Mode)			20	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	60			ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	65			ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	25			ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t _{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t _{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Read Mode)			2.5	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	180			ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t _{SOSU}	Time SO (SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t _{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

7. Command Table

Command Table																																																																			
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																							
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 127h [POR], 296 MUX MUX Gate lines setting as (A[8:0] + 1).																																																							
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																																									
0	1		0	0	0	0	0	0	0	A ₈																																																									
0	1		0	0	0	0	0	B ₂	B ₁	B ₀		B[2:0] = 000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ... B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...295 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G295 B[0]: TB TB = 0 [POR], scan from G0 to G295 TB = 1, scan from G295 to G0.																																																							
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 10V to 20V																																																							
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀		<table><tr><th>A[4:0]</th><th>VGH</th><th>A[4:0]</th><th>VGH</th></tr><tr><td>00h</td><td>20</td><td>0Dh</td><td>15</td></tr><tr><td>03h</td><td>10</td><td>0Eh</td><td>15.5</td></tr><tr><td>04h</td><td>10.5</td><td>0Fh</td><td>16</td></tr><tr><td>05h</td><td>11</td><td>10h</td><td>16.5</td></tr><tr><td>06h</td><td>11.5</td><td>11h</td><td>17</td></tr><tr><td>07h</td><td>12</td><td>12h</td><td>17.5</td></tr><tr><td>08h</td><td>12.5</td><td>13h</td><td>18</td></tr><tr><td>07h</td><td>12</td><td>14h</td><td>18.5</td></tr><tr><td>08h</td><td>12.5</td><td>15h</td><td>19</td></tr><tr><td>09h</td><td>13</td><td>16h</td><td>19.5</td></tr><tr><td>0Ah</td><td>13.5</td><td>17h</td><td>20</td></tr><tr><td>0Bh</td><td>14</td><td>Other</td><td>NA</td></tr><tr><td>0Ch</td><td>14.5</td><td></td><td></td></tr></table>	A[4:0]	VGH	A[4:0]	VGH	00h	20	0Dh	15	03h	10	0Eh	15.5	04h	10.5	0Fh	16	05h	11	10h	16.5	06h	11.5	11h	17	07h	12	12h	17.5	08h	12.5	13h	18	07h	12	14h	18.5	08h	12.5	15h	19	09h	13	16h	19.5	0Ah	13.5	17h	20	0Bh	14	Other	NA	0Ch	14.5	
A[4:0]	VGH	A[4:0]	VGH																																																																
00h	20	0Dh	15																																																																
03h	10	0Eh	15.5																																																																
04h	10.5	0Fh	16																																																																
05h	11	10h	16.5																																																																
06h	11.5	11h	17																																																																
07h	12	12h	17.5																																																																
08h	12.5	13h	18																																																																
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08h	12.5	15h	19																																																																
09h	13	16h	19.5																																																																
0Ah	13.5	17h	20																																																																
0Bh	14	Other	NA																																																																
0Ch	14.5																																																																		

Command Table															
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description			
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2			
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀					
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀					
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀					
A[7]/B[7] = 1, VSH1/VSH2 voltage setting from 2.4V to 8.8V															
A/B[7:0]				VSH1/VSH2				A/B[7:0]				VSH1/VSH2			
8Eh				2.4				AFh				5.7			
8Fh				2.5				B0h				5.8			
90h				2.6				B1h				5.9			
91h				2.7				B2h				6			
92h				2.8				B3h				6.1			
93h				2.9				B4h				6.2			
94h				3				B5h				6.3			
95h				3.1				B6h				6.4			
96h				3.2				B7h				6.5			
97h				3.3				B8h				6.6			
98h				3.4				B9h				6.7			
99h				3.5				BAh				6.8			
9Ah				3.6				BBh				6.9			
9Bh				3.7				BCh				7			
9Ch				3.8				BDh				7.1			
9Dh				3.9				BEh				7.2			
9Eh				4				BFh				7.3			
9Fh				4.1				C0h				7.4			
A0h				4.2				C1h				7.5			
A1h				4.3				C2h				7.6			
A2h				4.4				C3h				7.7			
A3h				4.5				C4h				7.8			
A4h				4.6				C5h				7.9			
A5h				4.7				C6h				8			
A6h				4.8				C7h				8.1			
A7h				4.9				C8h				8.2			
A8h				5				C9h				8.3			
A9h				5.1				CAh				8.4			
AAh				5.2				CBh				8.5			
ABh				5.3				CCh				8.6			
ACh				5.4				CDh				8.7			
ADh				5.5				CEh				8.8			
AEh				5.6				Other				NA			

A[7]/B[7] = 0, VSH1/VSH2 voltage setting from 9V to 17V															
A/B[7:0]				VSH1/VSH2				A/B[7:0]				VSH1/VSH2			
23h				9				3Ch				14			
24h				9.2				3Dh				14.2			
25h				9.4				3Eh				14.4			
26h				9.6				3Fh				14.6			
27h				9.8				40h				14.8			
28h				10				41h				15			
29h				10.2				42h				15.2			
2Ah				10.4				43h				15.4			
2Bh				10.6				44h				15.6			
2Ch				10.8				45h				15.8			
2Dh				11				46h				16			
2Eh				11.2				47h				16.2			
2Fh				11.4				48h				16.4			
30h				11.6				49h				16.6			
31h				11.8				4Ah				16.8			
32h				12				4Bh				17			
33h				12.2				Other				NA			
34h				12.4											
35h				12.6											
36h				12.8											
37h				13											
38h				13.2											
39h				13.4											
3Ah				13.6											
3Bh				13.8											

C[7] = 0, VSL setting from -5V to -17V															
C[7:0]				VSL											
0Ah				-5											
0Ch				-5.5											
0Eh				-6											
10h				-6.5											
12h				-7											
14h				-7.5											
16h				-8											
18h				-8.5											
1Ah				-9											
1Ch				-9.5											
1Eh				-10											
20h				-10.5											
22h				-11											
24h				-11.5											
26h				-12											
28h				-12.5											
2Ah				-13											
2Ch				-13.5											
2Eh				-14											
30h				-14.5											
32h				-15											
34h				-15.5											
36h				-16											
38h				-16.5											
3Ah				-17											
Other				NA											

0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
---	---	----	---	---	---	---	---	---	---	---	-------------------------------------	---

0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting

Command Table											Command	Description																												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																														
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting.																												
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[7:0] -> Soft start setting for Phase1 = 8Bh [POR]																												
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		B[7:0] -> Soft start setting for Phase2 = 9Ch [POR]																												
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		C[7:0] -> Soft start setting for Phase3 = 96h [POR]																												
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:0] -> Duration setting = 0Fh [POR]																												
												Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:																												
												<table><tr><th>Bit[6:4]</th><th>Driving Strength Selection</th></tr><tr><td>000</td><td>1(Weakest)</td></tr><tr><td>001</td><td>2</td></tr><tr><td>010</td><td>3</td></tr><tr><td>011</td><td>4</td></tr><tr><td>100</td><td>5</td></tr><tr><td>101</td><td>6</td></tr><tr><td>110</td><td>7</td></tr><tr><td>111</td><td>8(Strongest)</td></tr></table>	Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)										
Bit[6:4]	Driving Strength Selection																																							
000	1(Weakest)																																							
001	2																																							
010	3																																							
011	4																																							
100	5																																							
101	6																																							
110	7																																							
111	8(Strongest)																																							
												<table><tr><th>Bit[3:0]</th><th>Min Off Time Setting of GDR [Time unit]</th></tr><tr><td>0000 ~ 0011</td><td>NA</td></tr><tr><td>0100</td><td>2.6</td></tr><tr><td>0101</td><td>3.2</td></tr><tr><td>0110</td><td>3.9</td></tr><tr><td>0111</td><td>4.6</td></tr><tr><td>1000</td><td>5.4</td></tr><tr><td>1001</td><td>6.3</td></tr><tr><td>1010</td><td>7.3</td></tr><tr><td>1011</td><td>8.4</td></tr><tr><td>1100</td><td>9.8</td></tr><tr><td>1101</td><td>11.5</td></tr><tr><td>1110</td><td>13.8</td></tr><tr><td>1111</td><td>16.5</td></tr></table>	Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000 ~ 0011	NA	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5
Bit[3:0]	Min Off Time Setting of GDR [Time unit]																																							
0000 ~ 0011	NA																																							
0100	2.6																																							
0101	3.2																																							
0110	3.9																																							
0111	4.6																																							
1000	5.4																																							
1001	6.3																																							
1010	7.3																																							
1011	8.4																																							
1100	9.8																																							
1101	11.5																																							
1110	13.8																																							
1111	16.5																																							
												D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1																												
												<table><tr><th>Bit[1:0]</th><th>Duration of Phase [Approximation]</th></tr><tr><td>00</td><td>10ms</td></tr><tr><td>01</td><td>20ms</td></tr><tr><td>10</td><td>30ms</td></tr><tr><td>11</td><td>40ms</td></tr></table>	Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms																		
Bit[1:0]	Duration of Phase [Approximation]																																							
00	10ms																																							
01	20ms																																							
10	30ms																																							
11	40ms																																							
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control:																												
0	1		0	0	0	0	0	0	A ₁	A ₀																														
												<table><tr><th>A[1:0]</th><th>Description</th></tr><tr><td>00</td><td>Normal Mode [POR]</td></tr><tr><td>01</td><td>Enter Deep Sleep Mode 1</td></tr><tr><td>11</td><td>Enter Deep Sleep Mode 2</td></tr></table>	A[1:0]	Description	00	Normal Mode [POR]	01	Enter Deep Sleep Mode 1	11	Enter Deep Sleep Mode 2																				
A[1:0]	Description																																							
00	Normal Mode [POR]																																							
01	Enter Deep Sleep Mode 1																																							
11	Enter Deep Sleep Mode 2																																							
												After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver																												

0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A ₂	A ₁	A ₀		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.

0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect <table><tr><td>A[2:0]</td><td>VCI level</td></tr><tr><td>011</td><td>2.2V</td></tr><tr><td>100</td><td>2.3V</td></tr><tr><td>101</td><td>2.4V</td></tr><tr><td>110</td><td>2.5V</td></tr><tr><td>111</td><td>2.6V</td></tr><tr><td>Other</td><td>NA</td></tr></table> The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).	A[2:0]	VCI level	011	2.2V	100	2.3V	101	2.4V	110	2.5V	111	2.6V	Other	NA
A[2:0]	VCI level																									
011	2.2V																									
100	2.3V																									
101	2.4V																									
110	2.5V																									
111	2.6V																									
Other	NA																									
0	1		0	0	0	0	0	A ₂	A ₁	A ₀																
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh [POR]														
0	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
0	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.														
1	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
1	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] <table><tr><td>A[7:6]</td><td>Select no of byte to be sent</td></tr><tr><td>00</td><td>Address + pointer</td></tr><tr><td>01</td><td>Address + pointer + 1st parameter</td></tr><tr><td>10</td><td>Address + pointer + 1st parameter + 2nd pointer</td></tr><tr><td>11</td><td>Address</td></tr></table> A[5:0] – Pointer Setting B[7:0] – 1 st parameter C[7:0] – 2 nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.	A[7:6]	Select no of byte to be sent	00	Address + pointer	01	Address + pointer + 1st parameter	10	Address + pointer + 1st parameter + 2nd pointer	11	Address				
A[7:6]	Select no of byte to be sent																									
00	Address + pointer																									
01	Address + pointer + 1st parameter																									
10	Address + pointer + 1st parameter + 2nd pointer																									
11	Address																									
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.														

0	0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option <table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table> A[3:0] BW RAM option <table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table> B[7] Source Output Mode <table><tr><td>0</td><td>Available Source from S0 to S175</td></tr><tr><td>1</td><td>Available Source from S8 to S167</td></tr></table>	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content	0	Available Source from S0 to S175	1	Available Source from S8 to S167																				
0000	Normal																																																
0100	Bypass RAM content as 0																																																
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1	Available Source from S8 to S167																																																
0	1		B ₇	0	0	0	0	0	0	0	0																																						
0	0	22	0	0	1	0	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR) <table><tr><th>Operating sequence</th><th>Parameter (in Hex)</th></tr><tr><td>Enable clock signal</td><td>80</td></tr><tr><td>Disable clock signal</td><td>01</td></tr><tr><td> </td><td> </td></tr><tr><td>Enable clock signal → Enable Analog</td><td>C0</td></tr><tr><td>Disable Analog → Disable clock signal</td><td>03</td></tr><tr><td> </td><td> </td></tr><tr><td>Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal</td><td>91</td></tr><tr><td>Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal</td><td>99</td></tr><tr><td> </td><td> </td></tr><tr><td>Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal</td><td>B1</td></tr><tr><td>Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal</td><td>B9</td></tr><tr><td> </td><td> </td></tr><tr><td>Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC</td><td>C7</td></tr><tr><td>Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog →Disable OSC</td><td>CF</td></tr><tr><td> </td><td> </td></tr><tr><td>Enable clock signal →Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC</td><td>F7</td></tr><tr><td>Enable clock signal →Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC</td><td>FF</td></tr></table>	Operating sequence	Parameter (in Hex)	Enable clock signal	80	Disable clock signal	01			Enable clock signal → Enable Analog	C0	Disable Analog → Disable clock signal	03			Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal	91	Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal	99			Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal	B1	Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal	B9			Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC	C7	Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog →Disable OSC	CF			Enable clock signal →Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC	F7	Enable clock signal →Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC	FF
Operating sequence	Parameter (in Hex)																																																
Enable clock signal	80																																																
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0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																							
0	0	24	0	0	1	0	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0																																				
0	0																																																

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	1		0	1	0	0	A ₃	A ₂	A ₁	A ₀		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.
0	1		0	0	0	0	0	0	1	0		
0	1		0	1	1	0	0	0	0	1		

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0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1680 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈		
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode 2 F[6]: PingPong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not support for Display Mode 1
0	1		A ₇	0	0	0	0	0	0	0		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		
0	1		0	F ₆	0	0	F ₃	F ₂	F ₁	F ₀		
0	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀		
0	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀		
0	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
0	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀		

0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP																																				
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																						
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																						
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																																						
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																																						
0	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀																																						
0	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀																																						
0	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀																																						
0	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀																																						
0	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀																																						
0	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀																																						
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences																																				
0	1		0	0	0	0	0	0	A ₁	A ₀																																						
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HiZ. A [7:6] :Select VBD option <table><tr><td>A[7:6]</td><td>Select VBD as</td></tr><tr><td>00</td><td>GS Transition, Defined in A[2] and A[1:0]</td></tr><tr><td>01</td><td>Fix Level, Defined in A[5:4]</td></tr><tr><td>10</td><td>VCOM</td></tr><tr><td>11[POR]</td><td>HiZ</td></tr></table> A [5:4] Fix Level Setting for VBD <table><tr><td>A[5:4]</td><td>VBD level</td></tr><tr><td>00</td><td>VSS</td></tr><tr><td>01</td><td>VSH1</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11</td><td>VSH2</td></tr></table> A[2] GS Transition control <table><tr><td>A[2]</td><td>GS Transition control</td></tr><tr><td>0</td><td>Follow LUT (Output VCOM @ RED)</td></tr><tr><td>1</td><td>Follow LUT</td></tr></table> A [1:0] GS Transition setting for VBD <table><tr><td>A[1:0]</td><td>VBD Transition</td></tr><tr><td>00</td><td>LUT0</td></tr><tr><td>01</td><td>LUT1</td></tr><tr><td>10</td><td>LUT2</td></tr><tr><td>11</td><td>LUT3</td></tr></table>	A[7:6]	Select VBD as	00	GS Transition, Defined in A[2] and A[1:0]	01	Fix Level, Defined in A[5:4]	10	VCOM	11[POR]	HiZ	A[5:4]	VBD level	00	VSS	01	VSH1	10	VSL	11	VSH2	A[2]	GS Transition control	0	Follow LUT (Output VCOM @ RED)	1	Follow LUT	A[1:0]	VBD Transition	00	LUT0	01	LUT1	10	LUT2	11	LUT3
A[7:6]	Select VBD as																																															
00	GS Transition, Defined in A[2] and A[1:0]																																															
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00	LUT0																																															
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11	LUT3																																															
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀																																						
0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end A[7:0]= 02h [POR] <table><tr><td>22h</td><td>Normal.</td></tr><tr><td>07h</td><td>Source output level keep previous output before power off</td></tr></table>	22h	Normal.	07h	Source output level keep previous output before power off																																
22h	Normal.																																															
07h	Source output level keep previous output before power off																																															
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																						
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26																																				
0	1		0	0	0	0	0	0	0	A ₀																																						
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 15h																																				
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																						
0	1		0	0	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																						

0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h																																								
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																										
0	1		0	0	0	0	0	0	0	A ₈																																										
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																										
0	1		0	0	0	0	0	0	0	B ₈																																										
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table><tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>296</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table> A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table><tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>176</td></tr><tr><td>010</td><td>32</td><td>110</td><td>NA</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table> BUSY pad will output high during operation.	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	296	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	176	010	32	110	NA	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																																																	
000	8	100	128																																																	
001	16	101	256																																																	
010	32	110	296																																																	
011	64	111	NA																																																	
A[2:0]	Width	A[2:0]	Width																																																	
000	8	100	128																																																	
001	16	101	176																																																	
010	32	110	NA																																																	
011	64	111	NA																																																	
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀																																										
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table><tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>296</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table> A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table><tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>176</td></tr><tr><td>010</td><td>32</td><td>110</td><td>NA</td></tr><tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr></table> During operation, BUSY pad will output high.	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	296	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	176	010	32	110	NA	011	64	111	NA
A[6:4]	Height	A[6:4]	Height																																																	
000	8	100	128																																																	
001	16	101	256																																																	
010	32	110	296																																																	
011	64	111	NA																																																	
A[2:0]	Width	A[2:0]	Width																																																	
000	8	100	128																																																	
001	16	101	176																																																	
010	32	110	NA																																																	
011	64	111	NA																																																	
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀																																										
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].																																								
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																										
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].																																								
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																										
0	1		0	0	0	0	0	0	0	A ₈																																										
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.																																								

8.Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		$DS+(WS-DS)*n(m-1)$			8-3
T update	Image update time	at 25 °C		3	-	sec	
Life		Topr		1000000times or 5years			

Notes:

8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3 WS: White state, DS: Dark state

9. Handling, Safety and Environment Requirements

Warning	
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.	
Caution	
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module. Disassembling the display module can cause permanent damage and invalidates the warranty agreements. Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.	
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

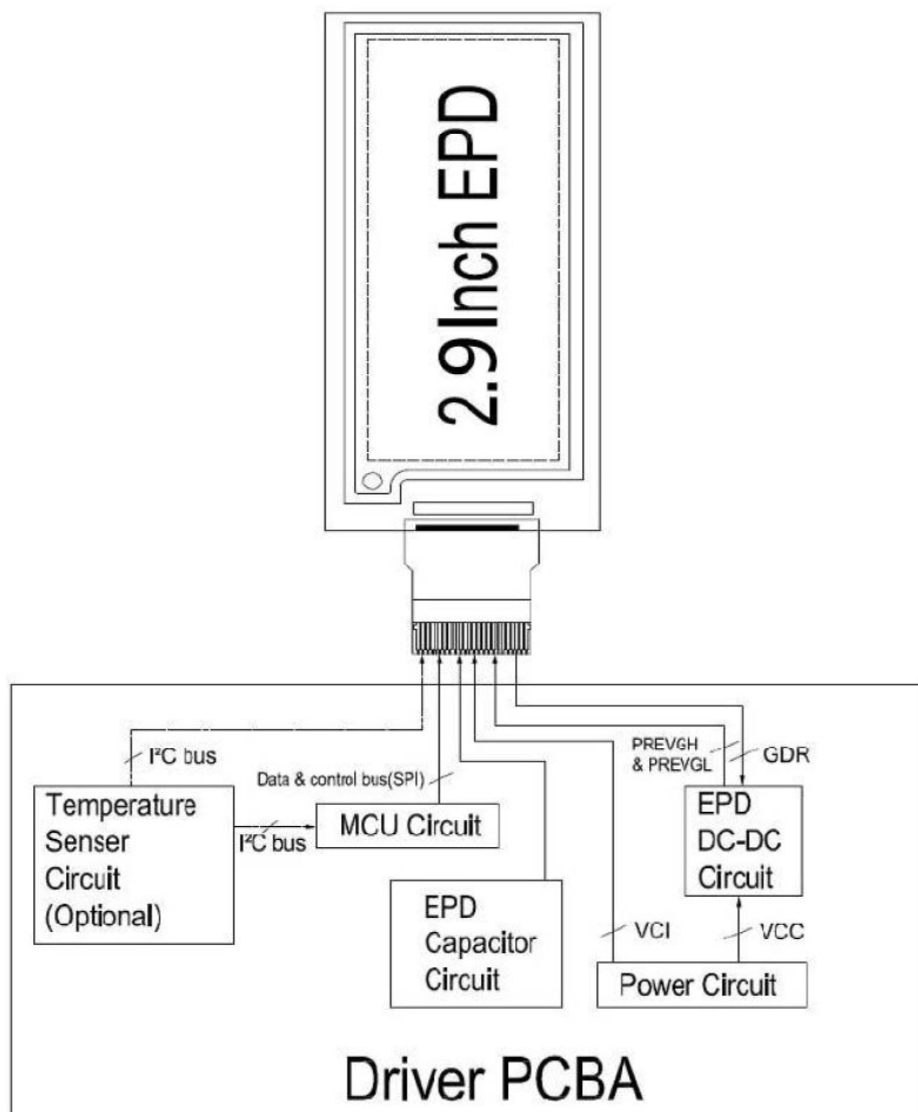
10. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70° C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=50° C, RH=35%, 240h
4	Low-Temperature Operation	0° C, 240h
5	High-Temperature, High-Humidity Operation	T=40° C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50° C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25° C 30min]→[+70 ° C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m ² for 168hrs, 40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

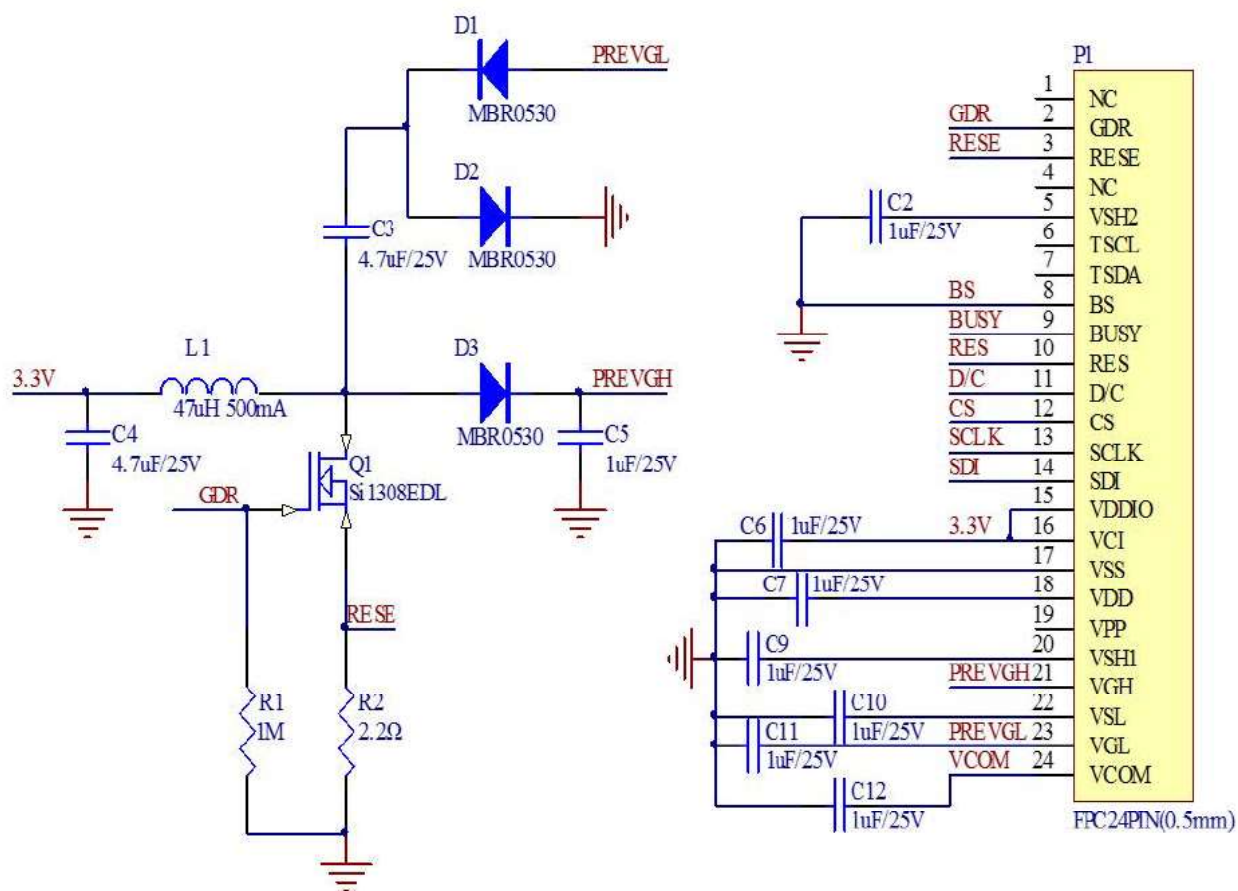
Note:

Put in normal temperature for 1hour after test finished, display performance is ok.

11. Block Diagram



12. Reference Circuit



13. Matched Development Kit

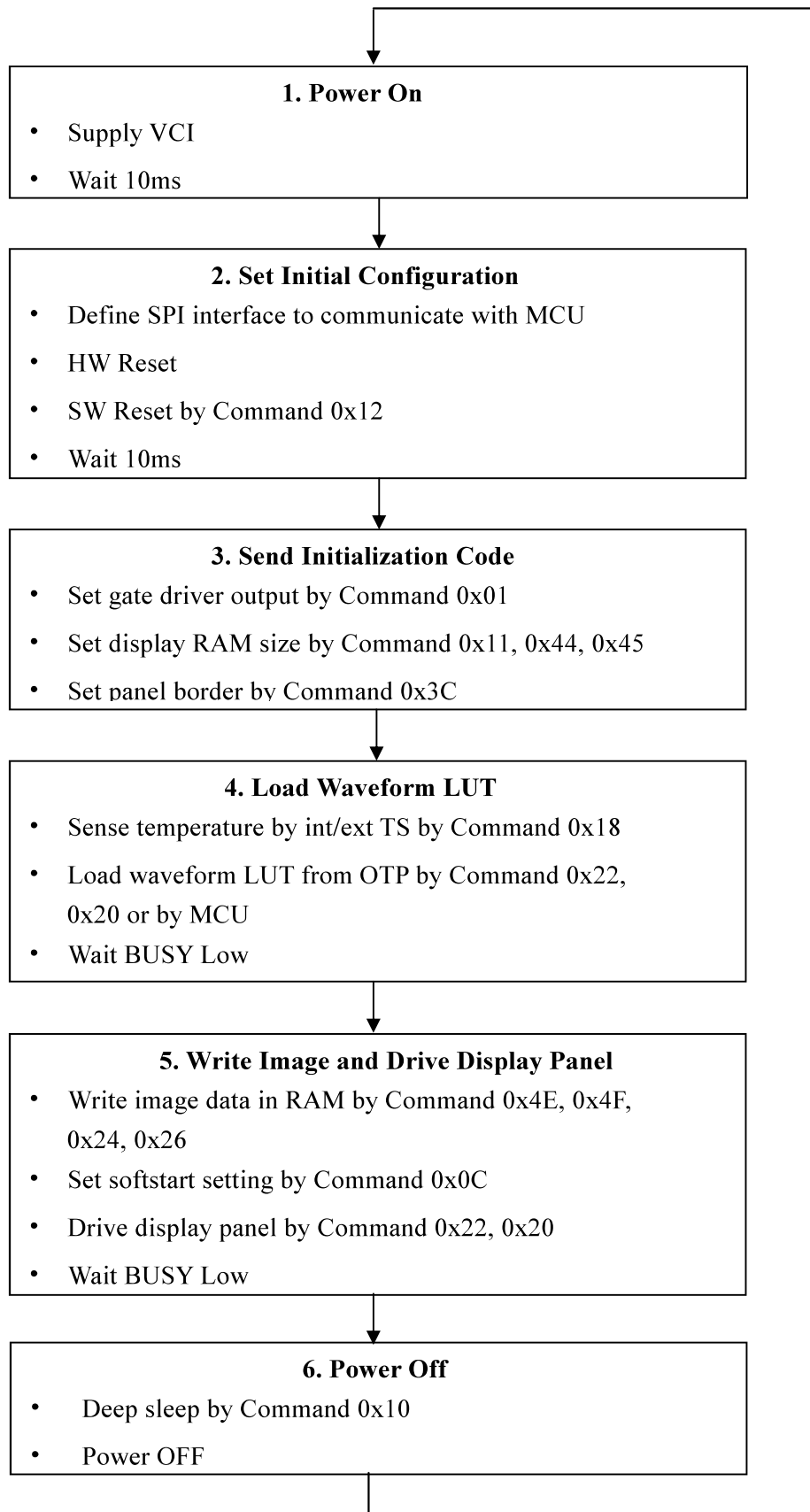
Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white

E-paper Display and three-color (black, white and red/Yellow) WINSTAR Display 's E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

DESPI Development Kit consists of the development board and the pinboard.

14. Typical Operating Sequence

14.1 Normal Operation Flow



15. Inspection condition

15.1 Environment

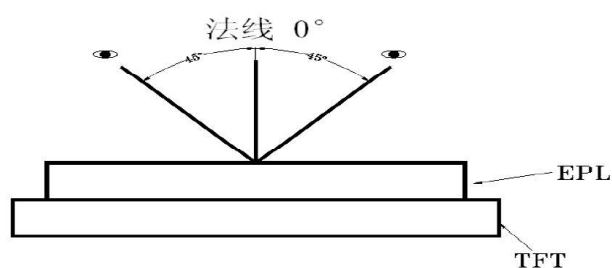
Temperature: $25 \pm 3^{\circ}\text{C}$

Humidity: $55 \pm 10\% \text{RH}$

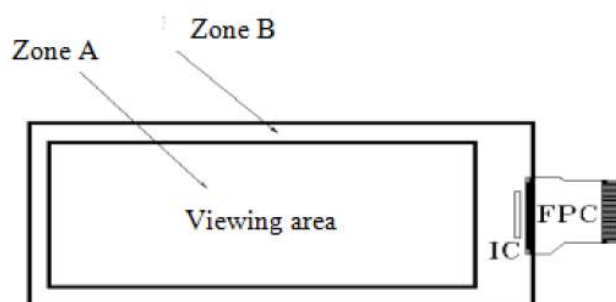
15.2 Illuminance

Brightness: 1200~1500LUX; distance: 20-30CM; Angle: Relate 30° surround.

15.3 Inspection method

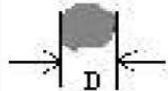
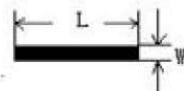


15.4 Display area

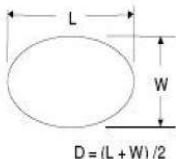
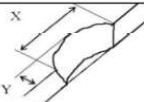
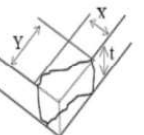
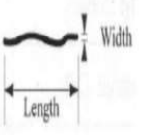


15.5 Inspection standard

15.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.25mm, Allowed 0.25mm < D≤0.4mm。N≤3, and Distance≥5mm 0.4mm < D Not Allow	MI		
3	Black/White spots (No switch)	 L≤0.6mm, W≤0.2mm, N≤1 L≤2.0mm,W>0.2mm, Not Allow L>0.6mm, Not Allow			
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow			

15.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 $D = (L + W) / 2$ $D \leq 0.25\text{mm}$, Allowed $0.25\text{mm} < D \leq 0.4\text{mm}$, $N \leq 3$ $D > 0.4\text{mm}$, Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 $X \leq 3\text{mm}, Y \leq 0.5\text{mm}$ And without affecting the electrode is permissible  $2\text{mm} \leq X$ or $2\text{mm} \leq Y$ Not Allow  $W \leq 0.1\text{mm}, L \leq 5\text{mm}$, No harm to the electrodes and $N \leq 2$ allow	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ Goldfingers oxidation/ scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: $X \leq 3\text{mm}$, $Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
9	PCB damaged/ Poor welding/ Curl	PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$	MI	Visual / Ruler	Zone B
10	Edge glue height/ Edge glue bubble	Edge Adhesives $H \leq$ PS surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 0.5\text{mm}$ 。 $n \leq 5$			
11	Protect film	Surface scratch but not effect protect function, Allowed		Visual Inspection	
12	Silicon glue	Thickness $\leq$ PS surface(With protect film); Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
13	Warp degree (TFT substrate)	$t \leq 2.0\text{mm}$	MI	Ruler	
14	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

16. Packing

TBD

17. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refresh the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.